

FIG. 1A PRIOR ART

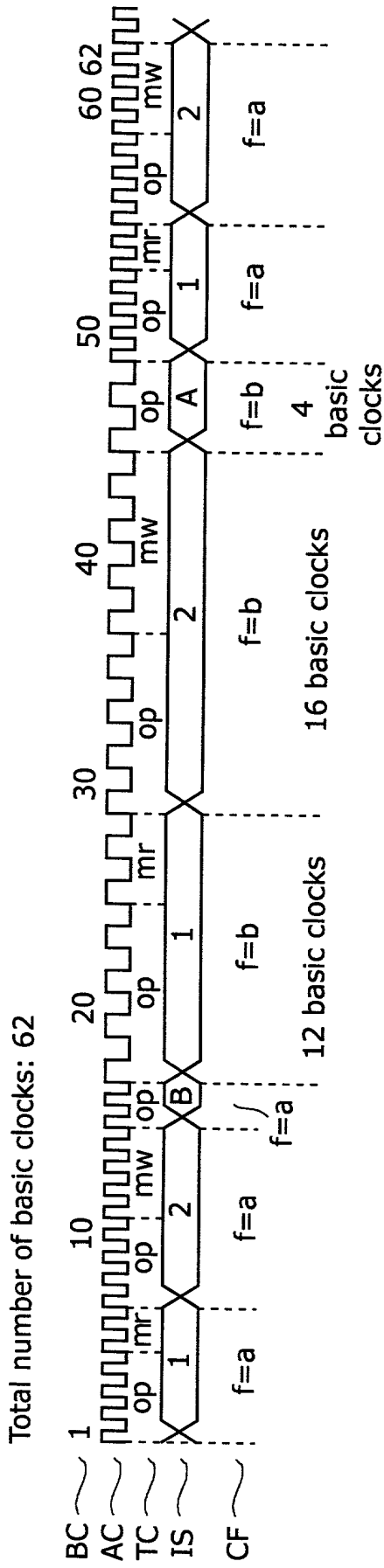


FIG. 1B

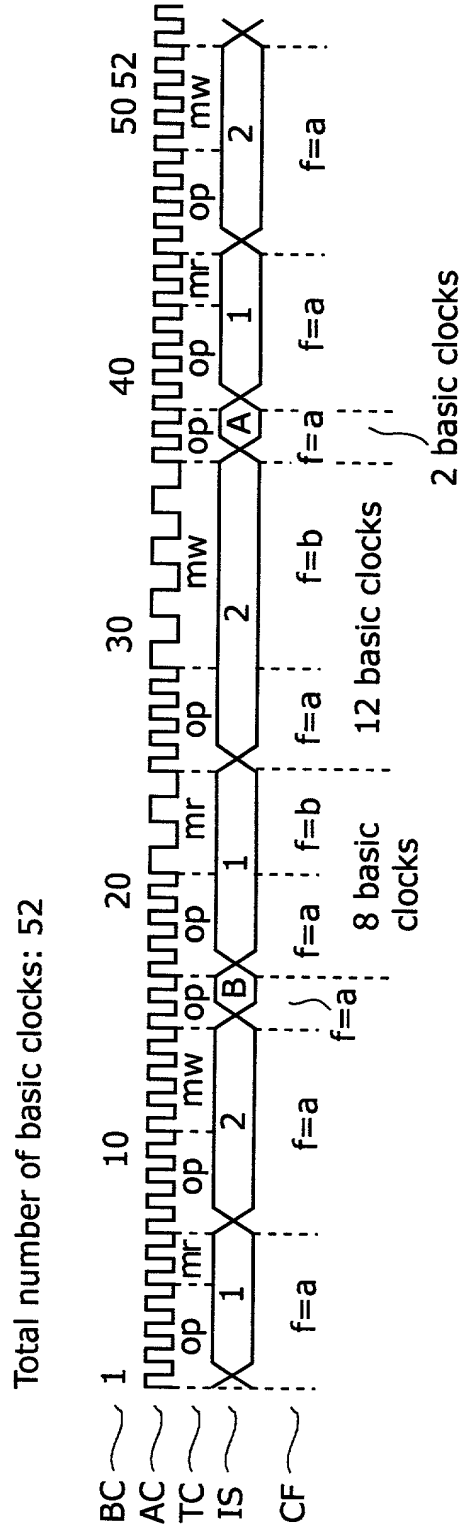


FIG. 2

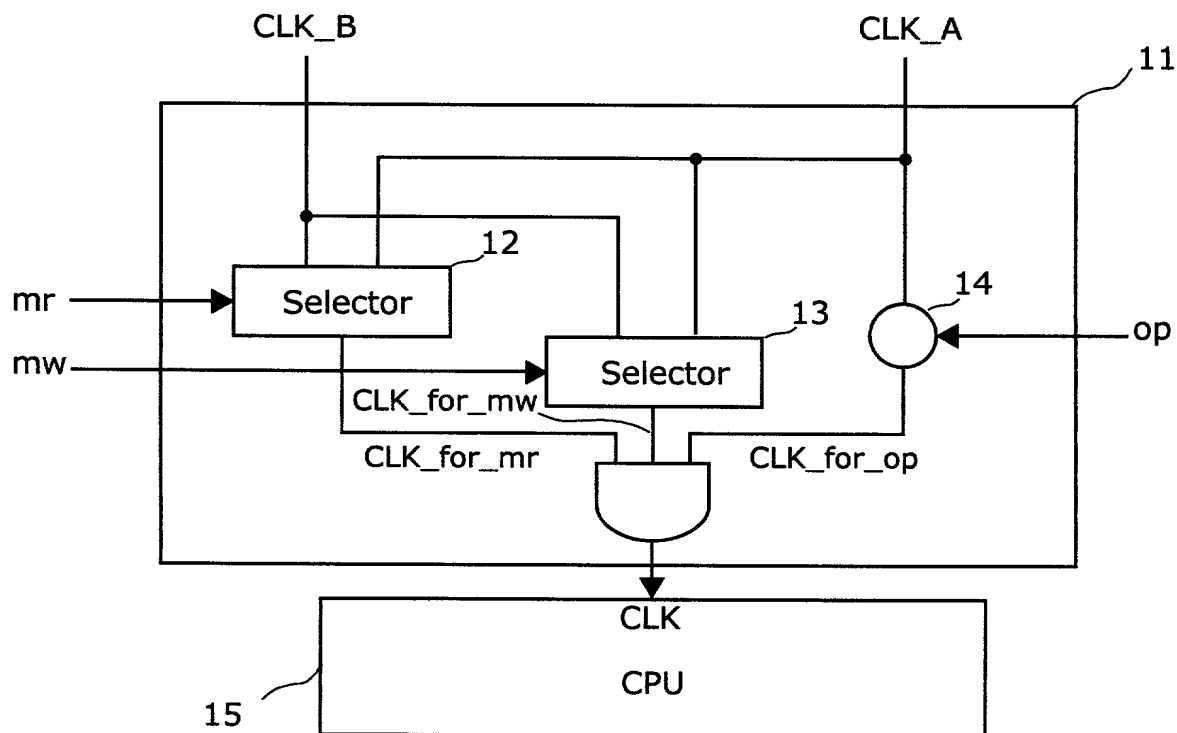


FIG. 3A

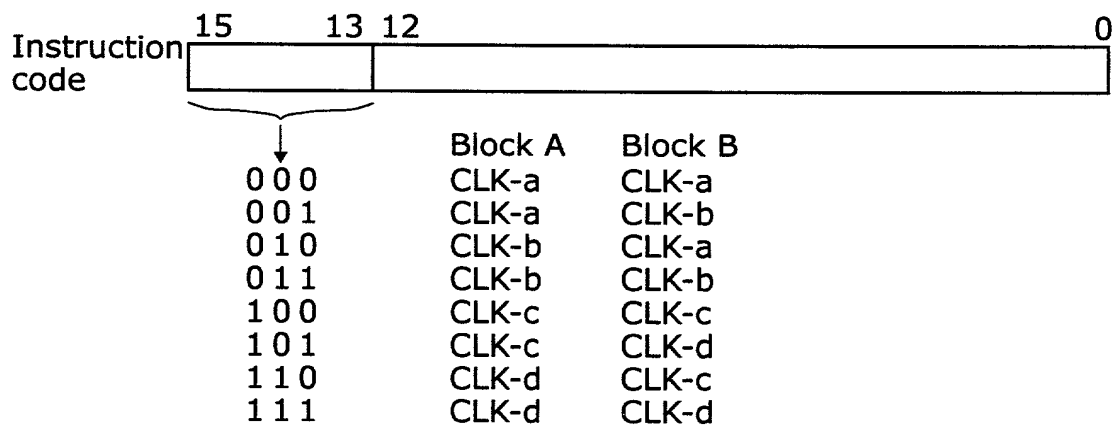


FIG. 3B

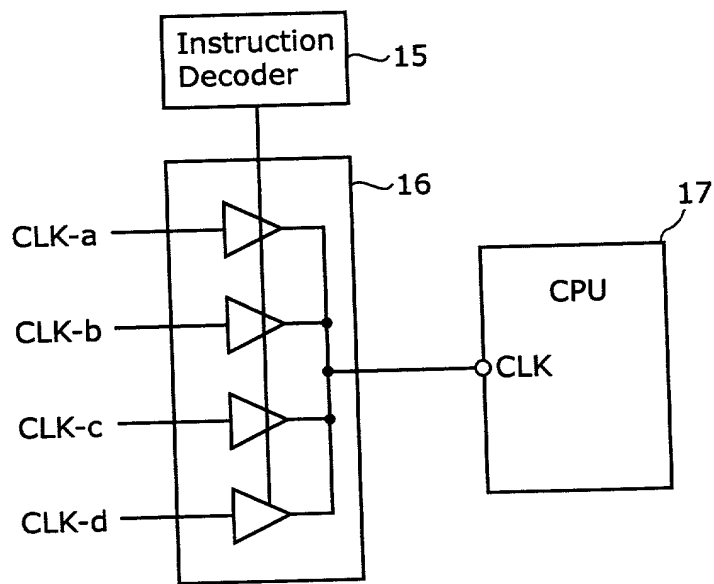


FIG. 3C

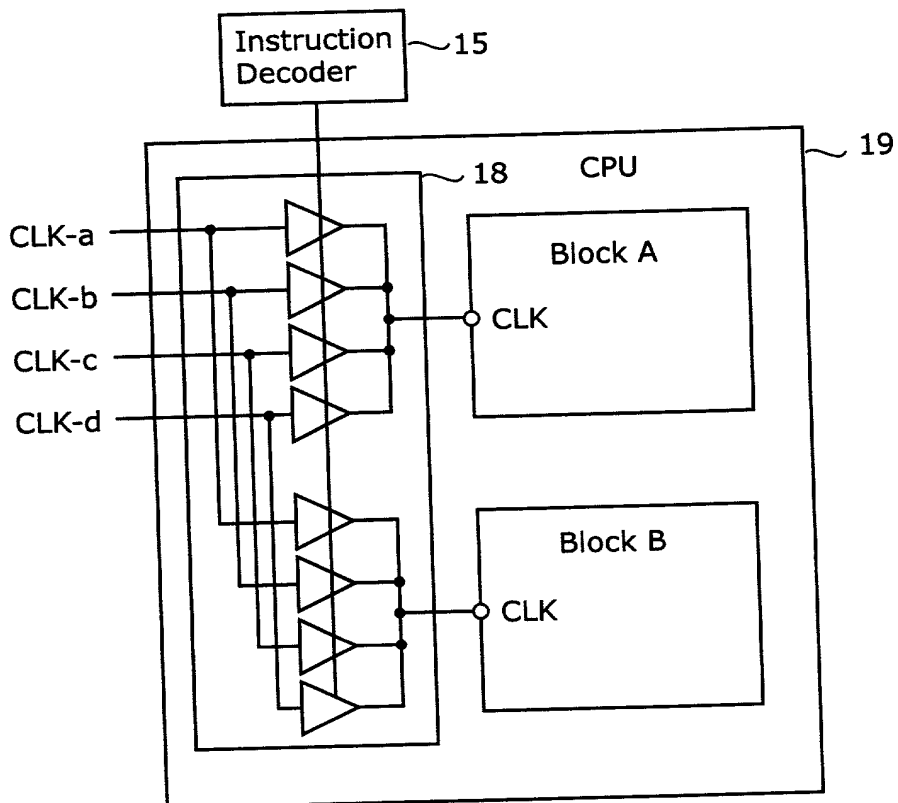


FIG. 4A

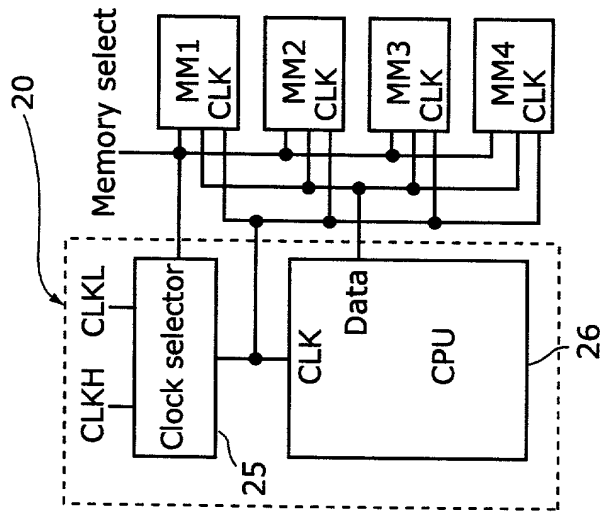


FIG. 4B

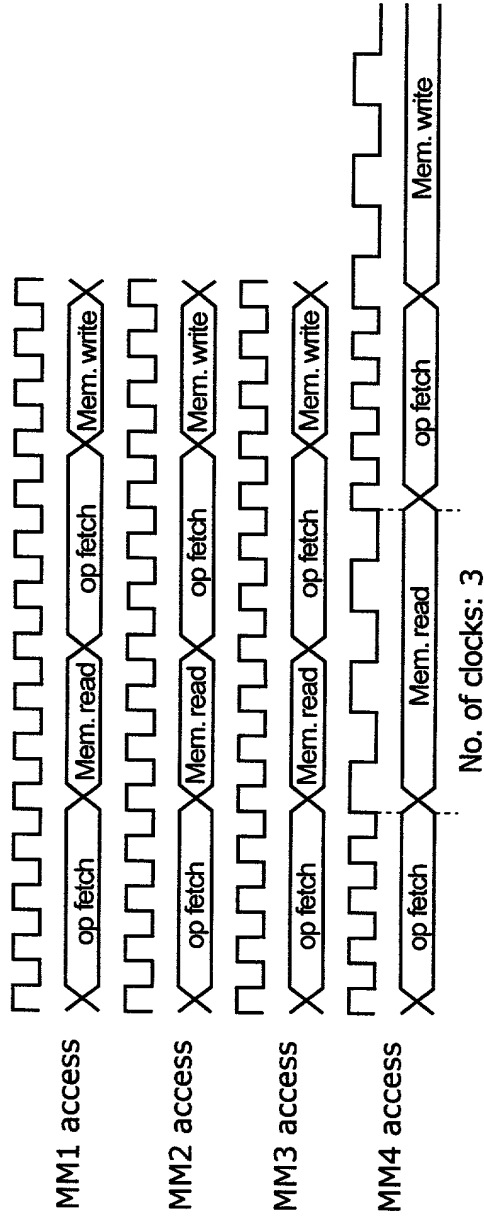


FIG. 4C

PRIOR ART

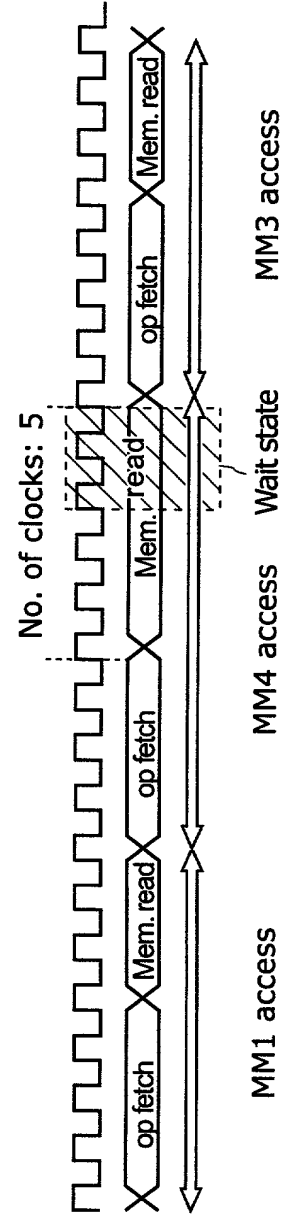


FIG. 5

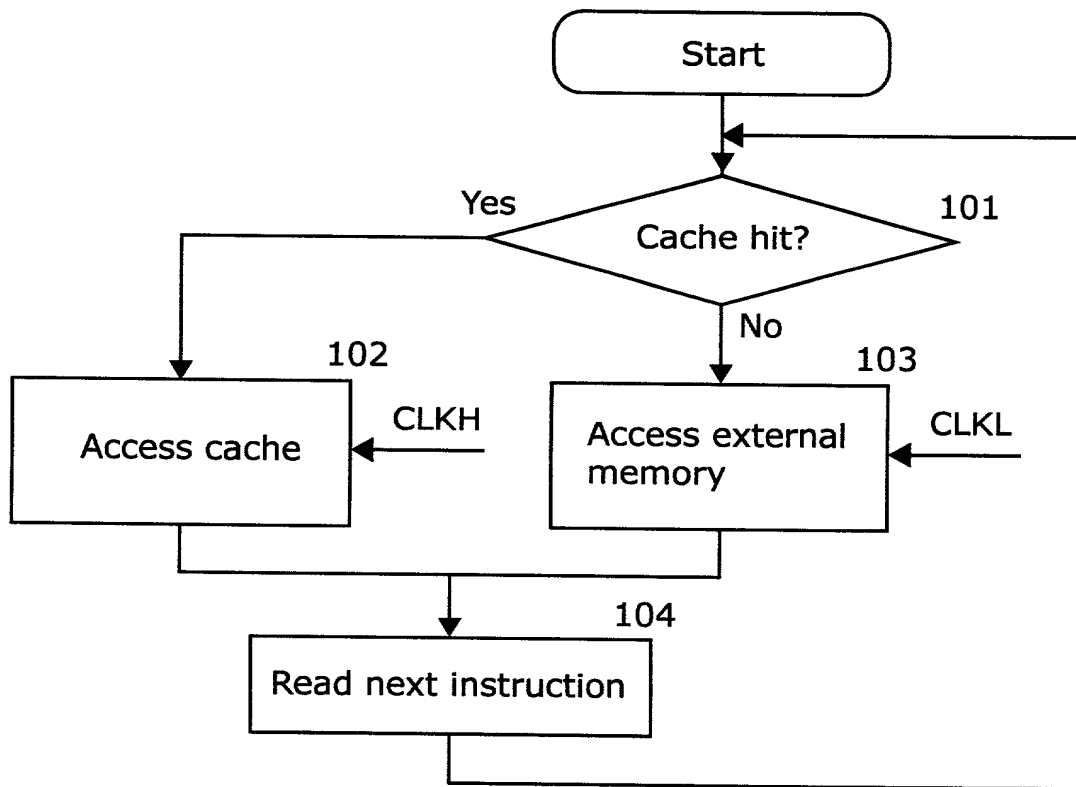


FIG. 6A PRIOR ART

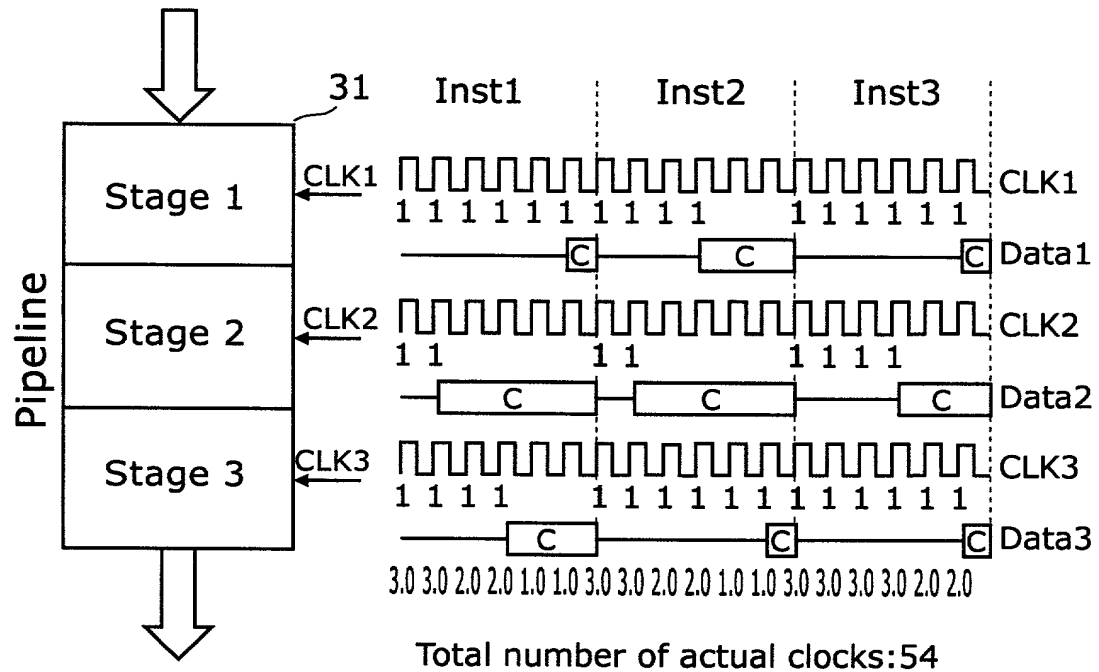


FIG. 6B

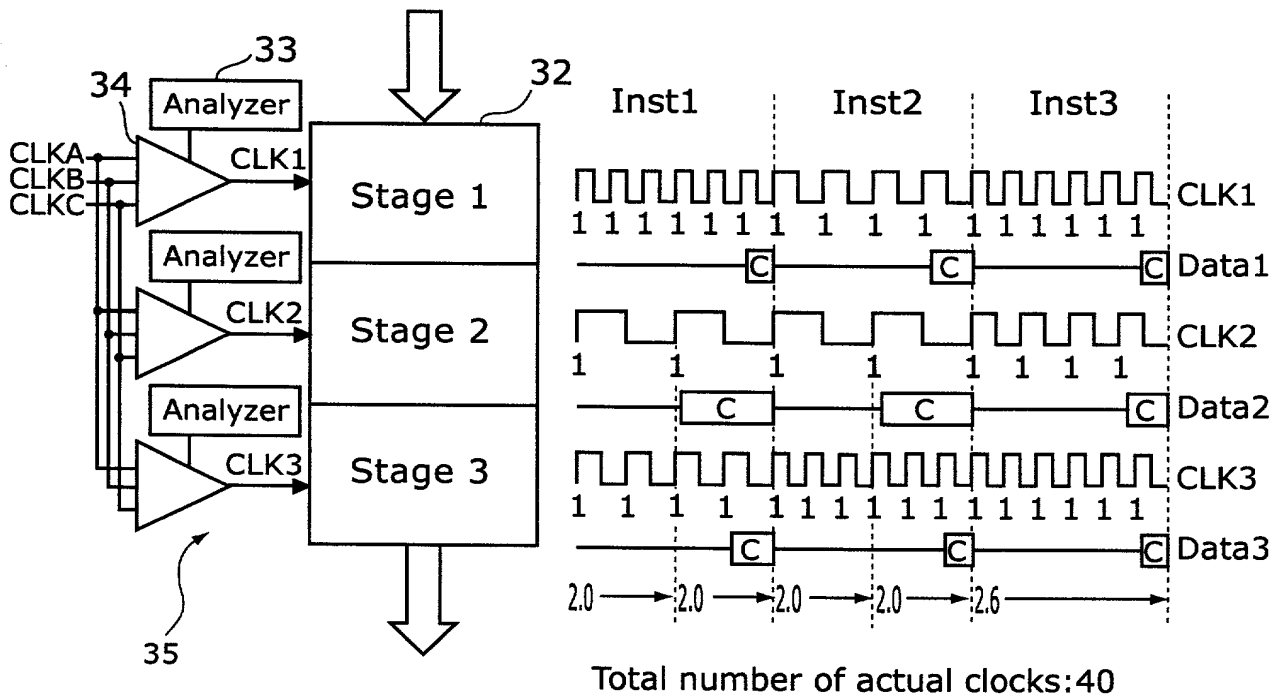


FIG. 7A

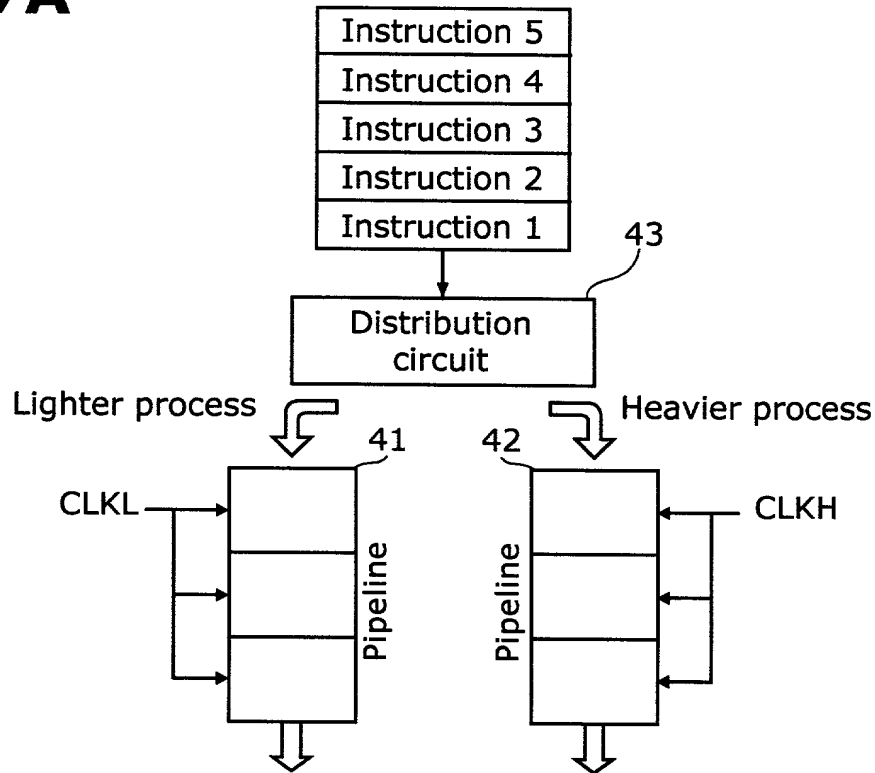


FIG. 7B

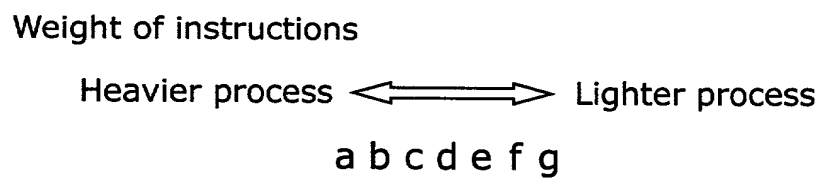


FIG. 7C

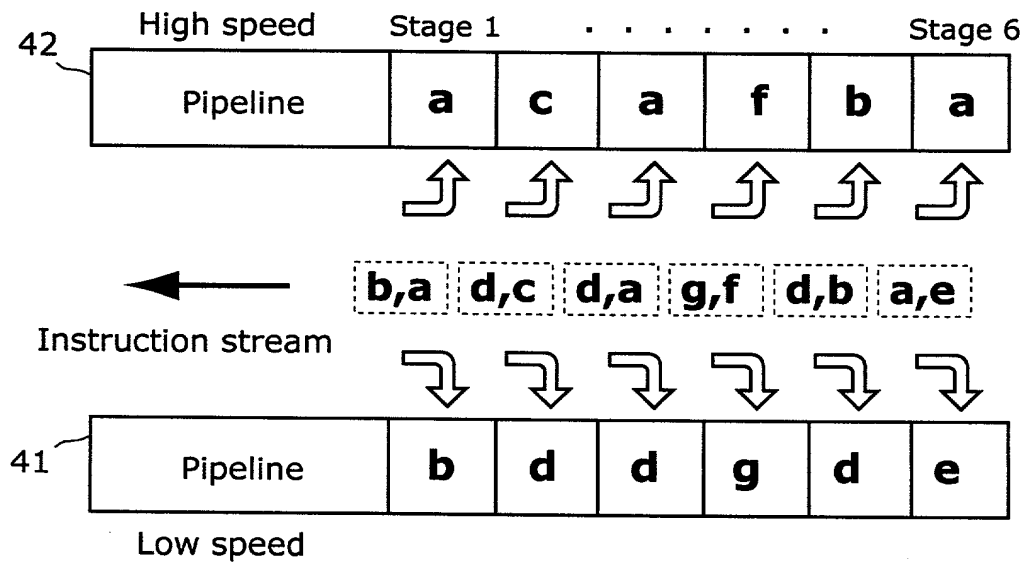


FIG. 8

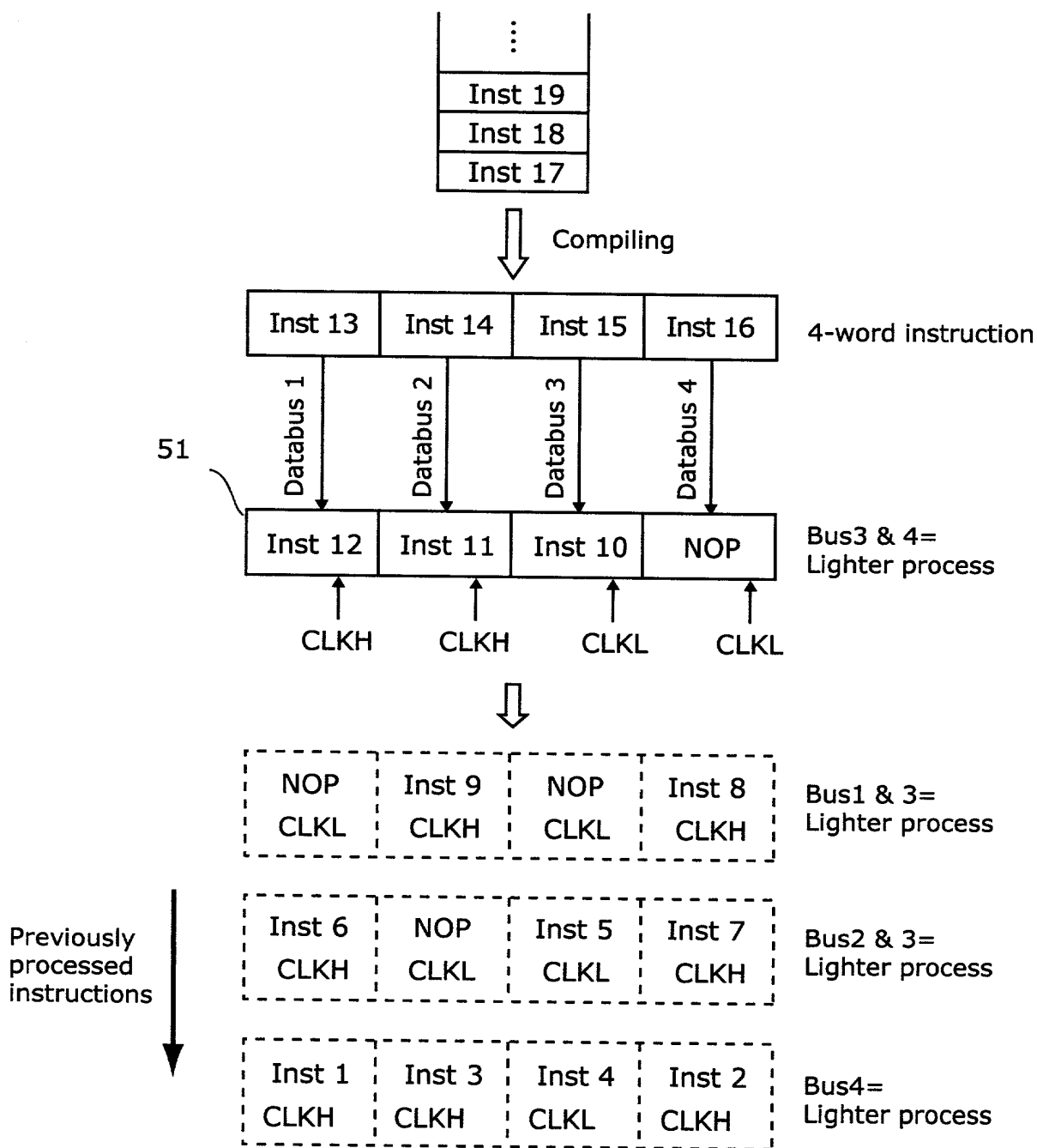


FIG. 9A PRIOR ART

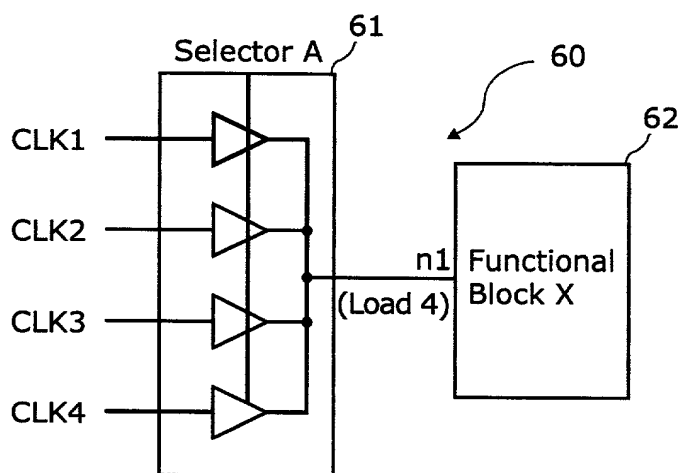


FIG. 9B

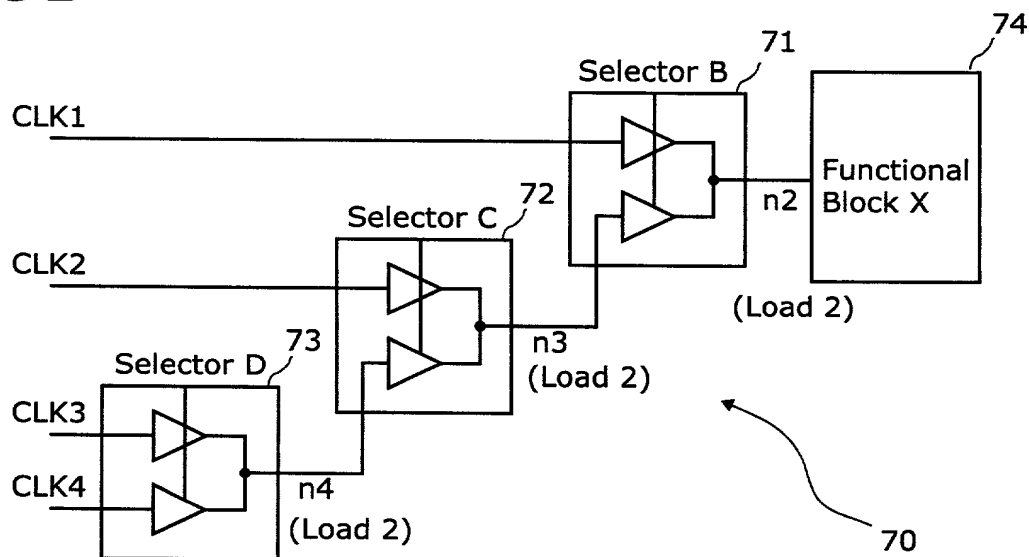


FIG. 9C

CLK Transition	CLK1	CLK2	CLK1	CLK2	CLK3
Clock selector block 60	4	4	4	4	4
Clock selector block 70	2	2	2	2	4

FIG. 10

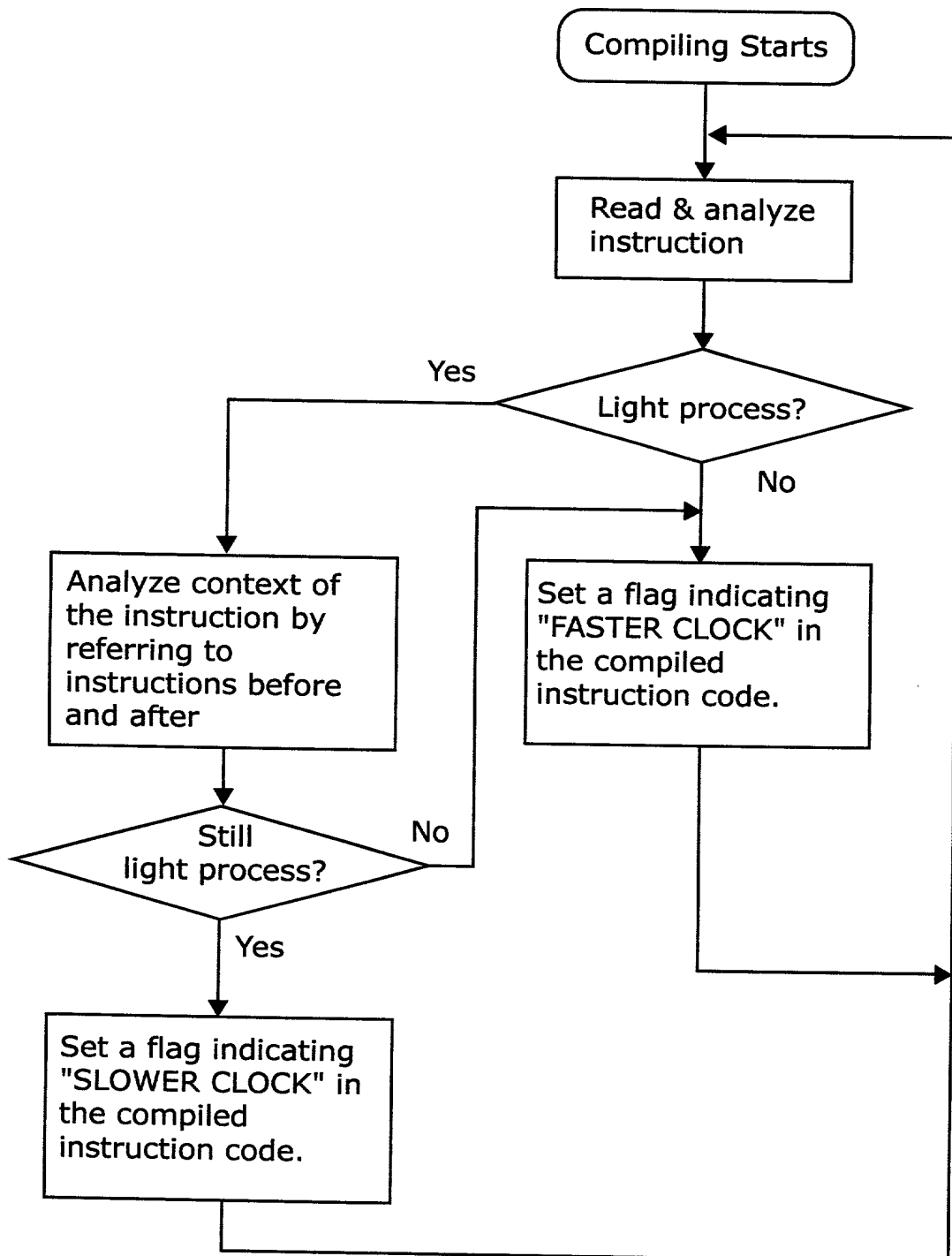


FIG. 11A **PRIOR ART**

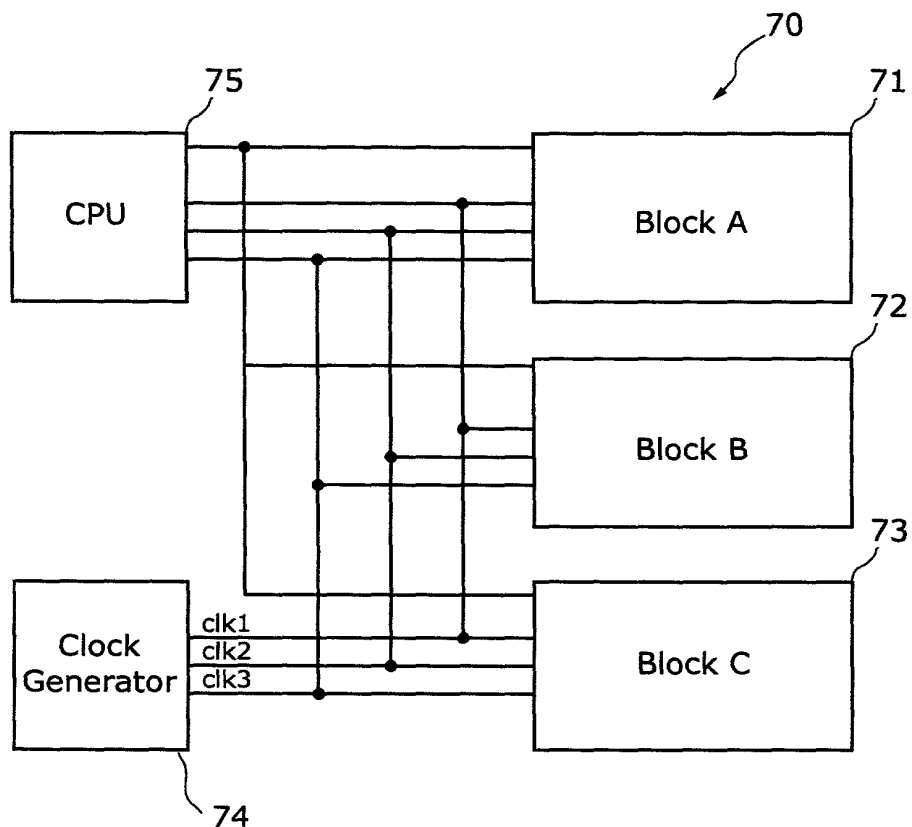


FIG. 11B **PRIOR ART**

Cycle	Block A	Block B	Block C
1	V		
2		V	
3	V		B
4	O	O	O
5		B	

V: Very active operation

O: Ordinally operation

B: Barely noticeable operation